COURSE STRUCTURE
AND
DETAILED SYLLABUS
(MR12Regulations)

for

M.Tech (VLSI System Design)
(Applicable for the batches admitted from 2012-13)

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

Maisammaguda, Dhulapally (PO) Via (Hakimpet), Hyderabad- 500 014.

www.mrec.ac.in **E-mail: mrec.2002@gmail.com**

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)
Maisammaguda, Dhulapally (Post via Hakimpet), Secunderabad – 500 014.

August/September 2012

Academic Regulations 2012 for M.Tech. (Regular)
(***Effective for the students admitted into first year from the academic year 2012-2013***)

The M.Tech Degree of Malla Reddy Engineering College, Hyderabad shall be conferred on candidates by the Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the university/college from time to time.

Admissions shall be made on the basis of merit rank obtained by the qualifying candidate at an Entrance Test conducted by the university/college or on the basis of any other order of merit approved by the university/college (say **PGECET / GATE)** subject to reservations prescribed by the university/college from time to time.

Candidates seeking admission to programmes on a part time basis should be working in or around the place where the programme is being run after passing qualifying examination.

2.0 AWARD OF M. TECH. DEGREE:

2.1 A student shall be declared eligible for the award of the M.Tech degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M.Tech course.

2.3 The minimum instruction for each semester 90 clear instruction days.

3.0 A. COURSE OF STUDY:

A candidate after securing admission must pursue the prescribed course of study for the following duration.

M.Tech - Four Semesters

Each Semester shall be of 22 Weeks of duration including examinations.

A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

The following specializations are offered at present for the M.Tech course of study..

1. Control Engineering
2. Computer Science and Engineering
3. Computer Science
4. Control Systems
5. Digital Systems & Computer Electronics
6. Structural Engineering
7. Thermal Engineering
8. Transportation Engineering
9. VLSI System Design

and any other course as approved by the authorities of the university/college from time to time.

Each subject is assigned certain number of credits depending upon the number of contact hours as follows.

Theory subjects	***4 Periods / Week***	***3 Credits***
Practical/ Drawing	***4 Periods / Week***	***2 Credits***
Seminar	***_***	***2 Credits***

Comprehensive Viva – Voce/ Independent Study 2 Credits
Project Work 40 Credits
(Each period will be of 50 minutes duration)

3.0 B. Departments offering M. Tech Programs with Specializations mentioned below:

Civil Engineering Department	1. Structural Engineering 2. Transport Engineering
Computer Science & Engineering Department	1. Computer Science & Engineering 2. Computer Science
Electrical Electronics Engineering Department	1. Control Systems 2. Control Engineering
Electronics & Communication Engineering Department	1. Digital Systems & Computer Electronics 2. VLSI System Design
Mechanical Engineering Department	1. Thermal Engineering

4.0 ATTENDANCE:
The programs are offered on a unit basis with each subject being considered unit.
4.1 A candidate shall be deemed to have eligibility to write end semester examinations in a subject if he has put in at least 65% of attendance in that subject.

4.2 ***Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%) may be condoned by the College Academic Committee on genuine and valid reasons on representation by the candidate with supporting evidence.***
4.3 A candidate shall get minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

4.4 ***Shortage of attendance below 65% shall in no case be condoned.***

4.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

5.0 EVALUATION:
The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination, 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the better of the marks secured in the two Mid Term-Examinations conducted one in the middle of the Semester and the other immediately after the completion of instruction each for a total of 30 marks. Each mid term examination shall be conducted for a duration of 120 minutes with 4 questions to be answered out of 6 questions. In addition, there shall be two assignments evaluated for 10 marks each and average of the two taken as the final assignment mark. The sum of the best of the two mid examinations and the assignment marks obtained shall be the final marks for internal evaluation.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations, 40 marks shall be awarded based on the day-to-day performance as internal Marks.
And 25 marks to be awarded by conducting an internal laboratory test. The End Examination shall be conducted by the teacher concerned and another faculty member of the same Department, as suggested by the Head of Department.

5.3 There shall be two seminar presentations during I year I semester and II Semesters. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the

Department, supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. *There shall be no external examination for Seminar*

5.4 Every candidate shall be required to execute his P.G. Project and submit his Dissertation, after taking up a topic approved by the Project Review Committee (PRC). The PRC shall be constituted by the Head of the Department, and shall consist of the Head of the Department, the Project supervisor, and a Senior faculty member of the Department. The PG project shall start immediately after completion of the I Year II Semester, and shall be of one year duration. The student has to decide his topic for his M.Tech Project Work within the first 6 weeks of the summer vacation at the end of the II semester and should submit his PG Project Work Proposal to the PRC, on whose approval he can register for the PG project. The PRC will monitor the progress of the project work through Two-Seminar presentations – one during II Year I Semester, and one before the submission of the PG Project/ Dissertation. The student shall submit a project Report at the end of that semester by the PRC as SATISFACTORY or UNSATISFACTORY. In the case of Unsatisfactory declaration, the student shall resubmit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC. The student can submit the Dissertation, only after completion of 40 weeks from the Date of Registration, after obtaining the approval from PRC. Extension of time, within the total permissible limit for the completion of the Degree, may be considered by the PRC, on sufficient valid/ genuine grounds.

5.5 There shall be a Seminar presentation in the II year I Semester, for the award of 50 marks. The seminar shall be on the topic chosen for PG Project/ Dissertation Work and the assessment will be done by the same PRC as constituted above. There shall be no external marks for the Seminar.

There shall be a Comprehensive Viva-Voce in II year II Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members in that area of specialisation. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studies during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 100 marks by the Committee. There are no internal marks for the Comprehensive viva-Voce

5.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.7 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and he has failed in the end examination. In such case candidate must re-register for the subject(s) and secure required minimum attendance. Attendance in the re-registered subject(s) has to be calculated separately to become eligible to write the end examination in the re-registered subject(s). The attendance of re-registered subject(s) shall be calculated separately to decide upon the eligibility for writing the end examination in those subject(s). In the event of taking another chance, the internal marks and end examination marks obtained in the previous attempt are nullified.

5.8 In case the candidate secures less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register the subject when next offered.

5.9 Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be other Laboratory Teacher or any other member from inside/outside of the college.

6.0 EVALUATION OF PROJECT/ DISSERTATION WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as chair person Heads of all the Departments which are offering the M.Tech programs and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Committee for its approval. Only after obtaining the approval of Departmental Committee the student can initiate the Project work. ***Departmental Committee Consists of Head of the Department as Chairman, along with two Senior Professors and few subject experts too.***

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 Candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation/demonstration before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College / School/ Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the College. For this, Head of the Department shall submit a panel of 5 examiners to the Principal of the College, who are eminent in that field with the help of the concerned guide and Head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report candidates work as:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree unless he is asked to revise and resubmit by the Board.

7.0 AWARD OF DEGREE AND CLASS:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured	*Program Credits*
First Class with Distinction	70% and above	***From the Aggregate secured for all the 88 credits***
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	
Pass Class	Below 50% but not less than 40%	

(The marks in internal evaluation and end examination shall be shown separately in the marks memorandum)

8.0 WITH-HOLDING OF RESULTS:

If the candidate has not paid any dues to the university or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to rule 5.5 and 2.0 of these regulations.

10.0 GENERAL:

10.1 The academic regulations should be read as a whole for purpose of any interpretation.

10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

10.3 The College may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the College.

10.4 Wherever the word he, him or his occur, it will also include she, her and hers.

10.5 Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject' and 'Practical Subject' or 'Lab'.

10.5 Transfers not allowed among group colleges.

MALLA REDDY ENGINEERING COLLEGE AUTONOMOUS-SECUNDERABAD-14
M.Tech. VLSI SYSTEM DESIGN
COURSE STRUCTURE AND SYLLABUS

I YEAR - I Semester

Code	Subject	L	T	P	Credits	Internal Assesme	External Assesme
MR124201	Digital IC Design (***)	3	1	0	3	40	60
MR124202	CPLD & FPGA Architectures and Applications	3	1	0	3	40	60
MR124203	VLSI Technology and Design	3	1	0	3	40	60
MR124204	Algorithms for VLSI Design Automation	3	1	0	3	40	60
MR124205 MR124206 MR124207	Microcontrollers for Embedded System Design Device Modeling MEMS	3	1	0	3	40	60
MR124208 MR124209 MR124210	Advanced Digital SignalProcessing Network Security &Cryptography Semiconductor Memory Design and Testing	3	1	0	3	40	60
MR124211	Simulation Lab	0		3	2	40	60
MR124212	Seminar I	-		-	2	50	
	Total Credits (6 Theory + 1 Lab.)				22	330	420

MALLA REDDY ENGINEERING COLLEGE AUTONOMOUS-SECUNDERABAD-14
M.Tech. VLSI SYSTEM DESIGN
COURSE STRUCTURE AND SYLLABUS

I YEAR - II Semester

Code	Subject	L	T	P	Credits	**Internal Assesme**	**External Assesme**
MR124213	CMOS Analog & Mixed Signal Design	3	1	0	3	40	60
MR124214	Low Power VLSI Design	3	1	0	3	40	60
MR124215	Digital Signal Processing and Architectures	3	1	0	3	40	60
MR124216	Design for Testability	3	1	0	3	40	60
MR124217 MR124218 MR124219	Hardware SoftwareCo-Design EROTS ASIC	3	1	0	3	40	60
MR124220 MR124221 MR124222	SOCA RF Circuit Design Genetic Algortihms & their Applications	3	1	0	3	40	60
MR124223	VLSI System Design Lab	0	0	3	2	40	60
MR124224	Seminar	-	-	-	2	50	
	Total Credits (6 Theory + 1				22	330	420

III SEMETER

Code	Subject	L	T	P	credits	End exam
MR124125	Comprehensive Viva	-	-	-	2	100
MR124126	Project Seminar	-	-	6	2	-
MR124127	Project work	-	-	-		-
	Total	-	-	6	4	100

IV SEMESTER

Code	Subject	L	T	P	credits	End Exam
MR124128	Project work & Seminar	-	-	-	40	Grade
	Grade (A/B/C/D)					A. Excellent B. Good C. Satisfactory D. Unsatisfactory

2012-2013 **Code MR124201**

MALLA REDDY ENGINEERING COLLEGE
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I Year – I Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

DIGITAL INTEGRATED CIRCUITS

UNIT I

Review Of Manufacturing Process: Issues In Digital Integrated Circuit Design, Quality Metrics Of Digital Design, Introduction, Manufacturing CMOS Integrated Circuits, Packaging Integrated Circuits.

Devices: Introduction, Diode, MOSFET Transistor, A Word On Process Variations, Perspective-Technology Scaling .

UNIT II

Wires And CMOS Inverter: Introduction, Interconnect Parameters- Capacitance, Resistance & Inductance, Electrical Wire Models, SPICE Wire Models, Introduction to CMOS Inverters, Static CMOS Inverter, Evaluating The Robustness Of The CMOS Inverter : The Static Behavior, Performance Of CMOS Inverter: The Dynamic Behavior, Power, Energy & Energy Delay, Perspective: Technology Scaling And Its Impact On The Inverter Metrics. Advanced Interconnect Techniques.

UNIT III

Designing Combinational Logic Gates In CMOS : Introduction , Static CMOS Design , Dynamic CMOS design Perspectives.

UNIT IV

Designing Sequential Logic Circuits : Introduction , Static Latches And Registers , Dynamic Latches And Registers, Alternative Registers Styles, Pipelining : An Approach To Optimize Sequential Circuits, Nonbistable Sequential Circuits, Perspectives: Choosing a Clocking Strategy , Cell - Based Design Methodology.

UNIT V

Timing Issues In Digital Circuits : Introduction, Timing Classification Of Digital Systems , Synchronous Design – An In depth Perspective , Self-Timed Circuit Design , Synchronizers And Arbiters .

Designing Arithmetic Building Blocks : Introduction , Datapaths In Digital Processor Architectures , The Adder, The Multiplier, The Shifter.

Text Books:

1. Digital Integrated Circuits (Second edition) : Jan M Rabaey , Anatha Chandrakasan, Borivoje Nikolic

2012-2013 **Code MR124202**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-III

Alternative realization for state machine chat suing microprogramming linked state machine one –hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT-IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") – Design flow using FPGAs

UNIT - V

Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

REFERENCES BOOKS :

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

2012-2013 **Code MR124203**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

VLSI TECHNOLOGY & DESIGN

UNIT – I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V:

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES BOOKS:

1. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

2012-2013 **Code MR124204**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I

PRELIMINARIES:Introduction to Design Methodologies, Design Automation tools, Algorithimic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION : Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming,Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

LAYOUT COMPACTION,PLACEMENT, FLOORPLANNING AND ROUTING: Problems, Concepts and Algorithms.

MODELLING AND SIMULATION:Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION:Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS:Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S & MCM'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.MCM technologies, MCM phsical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCES BOOKS :

1. Comoputer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

2012-2013 **Code MR1242015**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(ELECTIVE – I)

UNIT – I: Introduction to Embedded Systems

Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

UNIT – II: Microcontrollers and Processor Architecture & Interfacing

8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

UNIT – III: Embedded RISC Processors & Embedded System-on Chip Processor

PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

UNIT – IV: Interrupts & Device Drivers

Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

UNIT – V: Network Protocols

Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008,TMH.
2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.
3. Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

REFERENCES:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM Systems Developers Guides- Design & Optimizing System Software - Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

2012-2013 **Code MR1242016**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

DEVICE MODELLING
(ELECTIVE-I)

UNIT I:

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, continuity equation, Poisson equation

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, dependence of model parameters on structures

UNIT II:

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – static and dynamic behavior – small and large signal models – SPICE models

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, parasitic effects – SPICE model –parameter extraction

UNIT III:

Integrated MOS Transistor: nMOS and pMOS transistor – threshold voltage – threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT IV:

VLSI Fabrication Techniques: An overview of wafer fabrication, wafer processing – oxidation – patterning – diffusion – ion implantation – deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – interconnects circuit elements

UNIT V:

Modeling of Hetero Junction Devices: Band gap Engineering, Bandgap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid state circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd edition, Mcgraw hill, New York, 1981
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

2012-2013 **Code MR124207**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE-I)

UNIT –I

Introduction, basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT –II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, distributed force, distributed force, deflection curves for canti-levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – transient response of the MEMS.

UNIT – III

Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – IV

MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR<simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT – V

MEM Technologies: Silicon based MEMS- process flow – brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies. Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes. Status of MEMS in the current electronics scenario.

TEXT BOOKS:

1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley & Sons. .
2. Strength of Materials –Thimo Shenko, 2000, CBS publishers & Distributors.
3. MEMS and NEMS, Systems Devices; and Structures - Servey E.Lyshevski, 2002, CRC Press.

REFERENCE BOOKS:

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.

2012-2013 **Code MR124208**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-II)

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters.

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3 DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
3. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

2012-2013 **Code MR124209**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE-II)

UNIT-I

Introduction:Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques:

Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT-III

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.**Public Key Cryptography:**Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-IV

Number theoryPrime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Hash and Mac Algorithms:MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. **Digital signatures and Authentication protocols**: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT-V

Authentication Applications:Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.**IP Security:** Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. **Web Security:** Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.**Intruders, Viruses and Worms :** Intruders, Viruses and Related threats. **Fire Walls :** Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCE BOOKS:

1.Principles of Network and Systems Administration, Mark Burgess,John Wiel

2012-2013 **Code MR124210**

MALLA REDDY ENGINEERING COLLEGE
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I Year – I Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE-II)

UNIT I: Random Access Memory Technologies:

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, advanced DRAM design and architecture, Application specific DRAM

UNIT II: Non-volatile Memories:

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, nonvolatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT IV: Semiconductor Memory Reliability and Radiation Effects:

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliabilty, Reliabilty Test Structures, Reliabilty Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT V: Advanced Memory Technologies and High-density Memory Packing Technologies:

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:

1 Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2 Advanced Semiconductor Memories – Architecture, Design and Applications -Ashok K. Sharma-2002, Wiley.
3 Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu , 1st ed., Prentice Hall.

2012-2013 **Code MR124211**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – I Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	0	**-/3/-**	**3**

SIMULATION LAB (VLSI)

CYCLE 1:

1. Digital Circuits Description using Verilog.
2. Verification of the functionality of designed Circuits using function simulator.
3. Timing Simulation for critical Path time calculation.
4. Synthesis of Digital Circuits.
5. Place and route techniques for major FPGA Vendors using Xilinx, Altera, Cypress etc.,
6. Implementation of Designed Digital Circuits Using FPGA and CPLD devices.

CYCLE 2:

1. MOS inverter DC Characteristics, AC Characteristics, Transient Analysis.
2. NMOS, PMOS Characteristics.
3. Layout basics- INV, NAND, NOR, EXOR, EXNOR.
4. Layout of adder, subtractor, multiplexer.
5. Layout Comparator.

For Experiments in cycle 2: 3,4,5: Draw the Schematics Perform Simulation, Extract the Layout, Run Physical Verification (DRC, LVS, PEX) and post layout simulation.

2012-2013 **Code MR124212**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

CMOS ANALOG AND MIXED SIGNAL DESIGN

UNIT – I:

Current Sources & Sinks: The cascode connection, sensitivity and temperature analysis, transientresponse, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks.Voltage dividers, current source self-biasing, band gap voltage references, Beta-Multiplier ReferencedSelf-biasing.

UNIT – II:

Amplifiers: Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.

Feedback Amplifiers: Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

UNIT – III:

Differential Amplifiers: The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers, **Operational Amplifiers:** Basic CMOS Op-Amp Design, Operational Trans conductance Amplifiers, Differential Output Op-Amp.

MIXED SIGNAL CIRCUITS:

UNIT – IV:

Non-Linear & Dynamic Analog Circuits: Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

UNIT – V:

Data Converter Architectures: Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, 1st ed., TMH.

REFERENCES:

1. Analog Integrated Circuit Design – David A.Johns, Ken Martin, 1997, John-Wiley & Sons..
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor. C. Temes, John Wiley & Sons.

2012-2013 **Code MR124213**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – II Sem. M.Tech (VLSI System Design) **L T/P/D C**
3 -/-/- 3

LOW POWER VLSI DESIGN

UNIT I

Low Power Design - An over View: Introduction to low- voltage low power design, limitations, Siliconon-Insulator.MOS/BiCMOS Processes: Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT II

Low-Voltage/Low Power CMOS/ BiCMOS Processes: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT III

Device Behavior and Modeling: Advanced MOSFET models, limitations of MOSFET models, bipolar models.Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybridmode environment

UNIT IV

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and BiCMOS logic gates. Performance Evaluation

Low- Voltage Low Power Logic Circuits: Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation.

UNIT V

Low Power Latches And Flip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOK:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES:

1. Digital Integrated circuits - J.M.Rabaey, PH. N.J 1996
2. CMOS Digital Integrated Circuits Analysis & Design - Sung-MoKang, Yusuf Lleblebici 3rd ed., 2003, TMH 2003
3. VLSI DSP Systems – K.K. Parhi, 1999, John Wiley & Sons.
4. IEEE Trans Electron Devices, IEEE J, Solid State Circuits, and other National and International Conferences and Symposia.

2012-2013 **Code MR124214**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – II Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

DIGITAL PROCESSING PROCESSORS AND ARCHITECTURES

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT III

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

2012-2013 **Code MR124215**

MALLA REDDY ENGINEERING COLLEGE
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I Year – II Sem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
	3	**-/-/-**	**3**

DESIGN FOR TESTABILITY

UNIT – I

Introduction to Test and Design for Testability (DFT) Fundamentals

Modeling: Modeling Digital Circuits at Logic Level, register Level, and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation

UNIT – II

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault equivalence and Fault Location. Single Stuck and Multiple Stuck- Fault Models, Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT – III

Testing for Single Stuck Faults (SSF) – Automated Test Pattern Generation(ATPG/ATG) for SSFs in Combinational and Sequential Circuits, Functional Testing with Specific Fault Models, Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT – IV

Design for Testability – testability Trade-off's Techniques, Scan Architectures and Testing, Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells foe Scan Design, Board level and System level approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome test and Signature analysis.

UNIT – V

Built-in Self test (BIST) – BIST Concepts and Test pattern Generation. Specific BIST Architectures – LOCST, STUMPS, CBIST, RTD, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory Test Architectures and Techniques, Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test requirements for MBIST, JTAG Testing Features

TEXT BOOKS:

1. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breur, Arthu D.Friedman, John Wiley & Sons.
2 Design for Test for Digital ICs & Embedded Core Systems – Alfred Crouch, 2008, PE.
3. Introduction to VLSI Testing – Robrt.J.Feugate J, Steven M.Mclntyre, Englehood Cliffs, 1988, Prentice Hall.

REFERENCE BOOKS:

1. Essentials of Electronic Testing – M.L. Bushnell, Vishwani.D.Agarwal, Springer.

2012-2013 **Code MR124216**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – II Sem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

HARDWARE- SOFTWARE CO- DESIGN
(Elective – III)

UNIT –I

CO- DESIGN ISSUES :

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS :

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

PROTOTYPING AND EMULATION:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

TARGET ARCHITECTURES:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES:

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV

DESIGN SPECIFICATION AND VERIFICATION:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I

System – level specification, design representation for system level synthesis, system level specification languages,

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

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TEXT BOOKS :

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers

2012-2013 **Code MR124217**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

EMBEDDED REAL TIME OPERATING SYSTEMS
(ELECTIVE-III)

UNIT – I: Introduction

Introduction to UNIX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication,(pipes, fifos, message queues, semaphores, shared memory)

UNIT II: Real Time Systems:

Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

UNIT III: Scheduling & Inter-process Communication

Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling. Inter-process Communication and synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

UNIT IV: Real Time Operating Systems & Programming Tools

Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS EnvironmentMicro C/OS-II- Need of a well Tested & Debugged RTOs, Use of COS-II

UNIT V: VX Works & Case Studies

Memory managements task state transition diagram, pre-emptive priority, Scheduling context switchessemaphore- Binary mutex, counting watch dugs, I/O system Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using COS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

2012-2013 **Code MR124218**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

ASIC DESIGN
(ELECTIVE-III)

UNIT-I:

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture .

UNIT-II:

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT-III:

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX -Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT-IV:

ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floorplanning and Placement: Floorplanning- Placement- Physical Design Flow. Routing: Global Routing - Detailed Routing- Special Routing. Design checks

UNIT-V:

Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

TEXT BOOKS

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003

2012-2013 **Code MR124219**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

SYSTEM –ON-CHIP ARCHITECTURE
(ELECTIVE-IV)

UNIT I:

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor , Processor design trade off, Design for low power consumption

ARM Processor as System-on-Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface

UNIT II:

ARM Assembly Language Programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions

Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory

UNIT III:

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design- an example – memory management

UNIT IV:

Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture

UNIT V:

Architectural Support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output

TEXT BOOKS:

1. ARM System on Chip Architecture – Steve Furber – 2nd ed., 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st ed., 2004, Springer

REFERENCES:

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
2. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001,Kluwer Academic Publishers.

2012-2013 **Code MR124220**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

RF CIRCUIT DESIGN
(ELECTIVE-IV)

UNIT I: INTRODUCTION TO RF ELECTRONICS:

The Electromagnetic Spectrum, units and Physical Constants, Microwave bands – RF behavior of Passive components: Tuned resonant circuits, Vectors, Inductors and Capacitors -Voltage and Current in capacitor circuits – Tuned RF / IF Transformers.

UNIT II: TRANSMISSION LINE ANALYSIS

Examples of transmission lines-Transmission line equations and Biasing-Micro Strip Transmission Lines-Special Termination Conditions-sourced and Loaded Transmission Lines.

SINGLE AND MULTIPORT NETWORKS : The Smith Chart, Interconnectivity networks, Network properties and Applications, Scattering Parameters.

UNIT III: MATCHING AND BIASING NETWORKS

Impedance matching using discrete components – Micro strip line matching networks, Amplifier classes of Operation and Biasing networks

RF PASSIVE & ACTIVE COMPONENTS : Filter Basics – Lumped filter design – Distributed Filter Design – Diplexer Filters-Crystal and Saw filters-Active Filters -Tunable filters – Power Combiners / Dividers – Directional Couplers – Hybrid Couplers – Isolators. RF Diodes – BJTs-FETs-HEMTs and Models.

UNIT IV: RF TRANSISTOR AMPLIFIER DESIGN

Characteristics of Amplifiers -Amplifier Circuit Configurations, Amplifier Matching Basics, Distortion and noise products, Stability Considerations, Small Signal amplifier design, Power amplifier design, MMIC amplifiers, Broadband High Power multistage amplifiers, Low noise amplifiers, VGA Amplifiers

UNIT V: OSCILLATORS

Oscillator basics, Low phase noise oscillator design, High frequency Oscillator configuration, LC Oscillators, VCOs, Crystal Oscillators, PLL Synthesizer, and Direct Digital Synthesizer.

RF MIXERS : Basic characteristics of a mixer -Active mixers-Image Reject and Harmonic mixers, Frequency domain considerations.

TEXT BOOK:

1. RF circuit design: Theory and applications by Reinhold Ludwing, Pavel Bretchko. Pearson Education Asia Publication, New Delhi 2001

REFERENCE BOOKS:

1. Radio frequency and microwave electronics illustrated Mathew M. Radmangh, 2001,PE Asia Publication.
2. Secrets of RF Design by Joseph Carr., 3rd Edition, Tab Electronics
3. Complete Wireless Design by Cotter W. Sawyer, 2nd Edition, Mc-Graw Hill.
4. Practical RF Circuit Design for Modem Wireless Systems Vol.2 by Less Besser and Rowan Gilmore.

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2012-2013 **Code MR124221**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)

L	T/P/D	C
3	-/-/-	3

GENETIC ALGORITHMS AND THEIR APPLICATIONS
(ELECTIVE-IV)

UNIT I:
Fundamentals of genetic algorithm: A brief history of evolutionary computation-biological terminology-search space -encoding, reproduction-elements of genetic algorithm - genetic modeling - comparison of GA and traditional search methods.

UNIT II:
Steady state algorithm - fitness scaling - inversion, Genetic programming - Genetic algorithm in problem solving.

UNIT III:
Natural evolution -Simulated annealing and Tabu search .Genetic Algorithm in scientific models and theoretical foundations.

UNIT IV:
Computer implementation - low level operator and knowledge based techniques in Genetic Algorithm.

UNIT V:
Applications of Genetic based machine learning-Genetic Algorithm and parallel processors, composite laminates, constraint optimization, multilevel optimization, real life problem.

TEXT BOOKS

1. Melanie Mitchell, "An introduction to Genetic Algorithm", Prentice-Hall of India,New Delhi, Edition: 2004
2. David.E.Golberg, "Genetic algorithms in search, optimization and machine learning", Addision-Wesley-1999
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2012-2013 **Code MR124222**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

I Year – IISem. M.Tech (VLSI System Design)	**L**	**T/P/D**	**C**
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VLSI DESIGN LAB

NOTE: Following Experiments must be done using any one of the Back End Tools and all types of Analysis must be carried out(Transient, AC Analysis, DC Analysis, Post Lay out & Pre Layout Simulations etc)

Minimum 12 Experiments must be conducted

1. Current Source/Current Mirror Circuits
2. Common Source Amplifier
3. Class AB Amplifier with Load
4. Class AB Amplifier Without Load
5. Feed Back Amplifiers (Any two types among Four)
6. Differential Amplifier (Single Ended)
7. Trans conductance Operational Amplifier
8. CMOS as an Comparator
9. Analog Multiplier
10. Switched Capacitor Integrator
11. Switched Capacitor Common Mode Feedback Amplifier
12. Sample and Hold Circuit
13. Digital to Analog Converters (R-2R Ladder/Cyclic)
14. Analog to Digital Converters (SAR/Over Sampling etc)
15. Phase Locked Loop(Beyond the syllabus)